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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,653	01/24/2006	Koichi Kanaya	126247	6147
25944	7590	05/02/2007	EXAMINER	
OLIFF & BERRIDGE, PLC			CHEN, KEATH T	
P.O. BOX 19928			ART UNIT	PAPER NUMBER
ALEXANDRIA, VA 22320			1709	
			MAIL DATE	DELIVERY MODE
			05/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/565,653

Applicant(s)

KANAYA ET AL.

Examiner

Keath T. Chen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>10/5/2006, 01/24/2006</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Preliminary Amendment on 1/24/2006 by applicant is received. Claims 1-4 have been cancelled and claims 5-12 have been added and are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Van Bilsen et al. (US 6,284,048, hereafter '048).

'048 teaches all the limitations of claim 5:

A vapor phase growth apparatus (Fig. 1, #10) for performing a vapor phase growth of a silicon epitaxial layer (abstract) on a main surface (the top of #16 is a main surface) of a silicon single crystal substrate while heating the silicon single crystal substrate (Fig. 1, #16, epitaxial growth has to be on single crystal) placed on a pocket (Fig. 2, between #56 and #16) formed on a susceptor (#20), from both sides (Fig. 1, #13 and #14 are heaters), wherein the pocket has an outer peripheral side part (Fig. 2, #66) which supports a rear surface of the silicon single crystal substrate and an inner peripheral side part (Fig. 2, between #56 and #16) which is kept in a state of being more recessed than the outer peripheral side part in an inside of the outer peripheral side part, and the susceptor has a warped inverted U-shaped longitudinal sectional shape (Fig. 2, #62 is U-shaped, col.7, paragraph 3).

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3. Claims 5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by KOKUSAI DENKI (JP 2000355766 English Translation of detailed description, hereafter '766).

'766 teaches all limitations of claim 5:

A vapor phase growth apparatus (Fig. 3) for performing a vapor phase growth of a silicon ('766 translation, [0005]) epitaxial layer ([0001]) on a main surface of a silicon single crystal substrate while heating the silicon single crystal substrate (Fig. 3, #5, the top of #5 is a main surface) placed on a pocket (Fig. 2, #31) formed on a susceptor (Fig. 2, #17, the second susceptor), from both sides (Fig. 3, heating from left and right sides of each wafer #5), wherein the pocket has an outer peripheral side part (Fig. 2, the outside of #31 which is near the substrate #5) which supports a rear surface of the silicon single crystal substrate and an inner peripheral side part (Fig. 2, the inside of #31) which is kept in a state of being more recessed than the outer peripheral side part in an inside of the outer peripheral side part, and the susceptor has a warped inverted U-shaped longitudinal sectional shape (Fig. 2, #32, [0015]).

'766 further teaches the limitations of claim 7:

The susceptor is a type of a single wafer (Fig. 2, each secondary susceptor #17 holds one wafer #5), and a curvature on a rear surface side of the susceptor is $1.75 \times 10^{-5} \text{ mm}^{-1}$ or less.

Based on the information in Table 1 of '766, an 8 inch wafer with an 85 μm depth crevice is equivalent to a curvature of $1.7 \times 10^{-5} \text{ mm}^{-1}$, therefore, '766 anticipated the limitations of claim 7.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over '048, in view of Yao et al. (US 2002/0066412, hereafter '412).

'048 teaches all limitations of claim 5, as discussed above. '048 further teaches the distance between a bottom surface of the inner peripheral side part in the pocket and a rear surface of the silicon single crystal substrate (or the gap) for 200 mm wafers (col. 7, line 41-48) can be between 0.005 and 0.080 inch (between 0.127 mm and 2.03 mm). '048 further recognizes application for 300 mm wafer (col. 8, lines 1-3).

'048 does not explicitly teaches the gap size for a 300 mm or more wafer, particularly does not express a maximum distance of gap is less than 0.4 mm.

'412 is an analogous art in the field of chemical vapor deposition, specifically for processing a semiconductor substrate that minimizes contact with the backside of the

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substrate. '412 provides the gap depth at a range of 0.15 to 0.5 mm for 300 mm wafers (bottom of [0029]), preferably at 0.25 mm.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to have adopted the range provided by '412 and incorporated a 0.25 mm gap depth to be the pocket depth in Fig. 2 of '048 (same as the thickness of the lips #66), in a susceptor for 300 mm wafers, with a reasonable expectation of success and the expectation of similar results. The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945) (MPEP 2144.07).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over '048 as applied to claim 5, and further in view of Dutartre et al. (US 6162706, hereafter '706).

'048 teaches all the limitation of claims 5, as discussed above.

'048 does not teach the limitation of claim 9:

A vapor phase growth method, comprising performing a vapor phase growth of a silicon epitaxial layer on a main surface of a silicon single crystal substrate using the vapor phase growth apparatus as claimed in claim 5.

'706 is an analogous art in the vapor phase epitaxial deposition of silicon on a silicon substrate. '706 teaches a vapor phase growth method, comprising performing a vapor phase growth of a silicon epitaxial layer on a main surface of a silicon single crystal substrate (abstract).

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At the time of the invention was made, it would have been obvious to one having ordinary skill in the art to have known that the method performed in '706 is capable of being performed by the apparatus as taught by '408, given the fact that '706 is a vapor phase method of forming an epitaxial layer of Si on top of a single crystal Si substrate and a suitable apparatus for performing said step would be the device as taught in '408. The motivation would have been to achieve a reduced temperature ramp time by using a lower mass susceptor.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over '048 and '412 as applied to claim 6 above, and further in view of '706, for the same reasons given regarding claim 9 above.

7. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over '766, in view of '412.

'766 teaches all limitations of claim 5 and 7, as discussed above. '766 further teaches the distance between a bottom surface of the inner peripheral side part in the pocket and a rear surface of the silicon single crystal substrate (or the gap) for 200 mm wafers. Although '766 indicates the depth of the gap increases as wafer size increases, the gap depth is well below 0.4 mm (Table 1).

'766 does not explicitly teaches the gap size for a 300 mm or more wafer, and a maximum distance of gap is less than 0.4 mm.

'412 is an analogous art in the field of chemical vapor deposition, specifically for processing a semiconductor substrate that minimizes contact with the backside of the

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substrate. '412 provides the gap depth at a range of 0.15 to 0.5 mm for 300 mm wafers (bottom of [0029]), preferably at 0.25 mm.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to have adopted the range provided by '412 and incorporated a 0.25 mm gap depth to the pocket #31 in Fig. 2 of '766, in a susceptor for 300 mm wafers, with a reasonable expectation of success and the expectation of similar results. The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945) (MPEP 2144.07).

8. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over '766 as applied to claims 5 and 7 above (numerate list item 3), and further in view of '706, for the same reasons given regarding claim 9 above (numerate list item 5).

9. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over '766 and '412 as applied to claims 6 and 8 above (numerate list item 7), and further in view of '706, for the same reasons given regarding claim 9 above (numerate list item 5).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keath T. Chen whose telephone number is 571-270-1870. The examiner can normally be reached on M-F, 8:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Cleveland can be reached on 571-272-1418. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

kc

K.C.


MICHAEL B. CLEVELAND
SUPERVISORY PATENT EXAMINER